An Analysis of Single Event Upset Dependencies on High Frequency and Architectural Implementations within Actel RTAX-S Family Field Programmable Gate Arrays

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***Abstract*—In order to investigate frequency and architectural effects on Single Event Upset cross sections within RTAX-S FPGA devices, a novel approach to high speed testing is implemented. Testing was performed at variable speeds ranging from 15 MHz to 150 MHz.**

***Index Terms*—Actel, anti-fuse, FPGA, high frequency, single event upsets, TMR, transients.**

I. Introduction

THE Actel RTAX-S family consists of radiation hardened anti-fuse based Field Programmable Gate Arrays (FPGAs). Triple mode Redundancy (TMR) is the mitigation scheme implemented at each flip-flop or DFF (referred to as RCELL—a TMR'd DFF). Limitations exist for this method of mitigation and are mostly evident during high frequency operation [1]. Due to the number of transistors contained in an RCELL, there exist several points of possible fault capture (i.e., a Single Event Transient (SET) becoming a Single Event Upset (SEU)). Within each RCELL the DFF is tripled, however, all 3 DFFs share the same data, clock, enable, and reset lines [2]. Due to this fact, a glitch appearing on one of these lines during a clock edge will most likely appear as the same value to all of the DFFs and will not be correctly mitigated [3]. Fig. 1 is a high-level schematic representation of an Actel TMR'd DFF primitive. As an additional caveat, each RCELL has an enable MUX that is also shared between the tripled DFFs. If this MUX cell generates an SET, it may be caught by its associated DFF. As the system clock frequency is increased, so is the probability of capturing the SET. As the number of levels of combinatorial logic between each DFF increases, the probability of generating a SET increases. Based on these phenomena and novel testing methods, this paper presents the first high frequency radiation effects analysis for the RTAX-S series of devices.

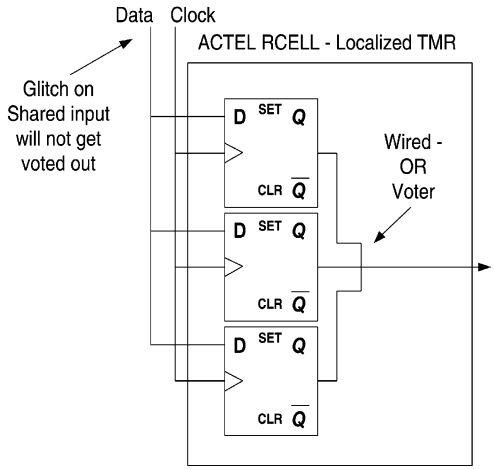

Fig. 1. Actel RCELL DFF Primitive.

II. Design Under Test

The objective of the testing was to analyze the frequency and architectural dependencies of SEU susceptibility within the RTAX-S family of devices. Therefore one of the requirements of the Design Under Test (DUT) was to be operable within a wide range of input clock frequencies. The upper bound was chosen to be 150 MHz. Such a bound limits the amount of combinatorial logic that can be placed between the DUT DFFs in order to avoid critical path timing violations.

The test structure consisted of shift register strings along with a novel architecture for capturing high-speed data (described later). In order to analyze architectural dependencies, various levels of combinatorial logic (inverter strings) were placed between DFF data input ports [1], [9] and combinatorial logic was placed at the DFF enable pins (mimicking fan-out). Various numbers of DFFs per shift register string were also analyzed to

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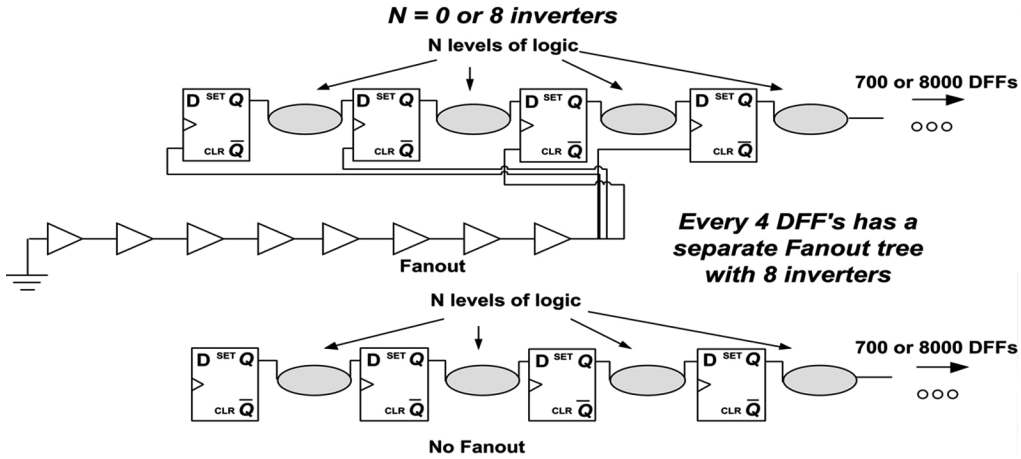

Fig. 2. RTAX-S Architecture Chains.

TABLE I
DUT TECHNOLOGY

Manufacturer	DUT	LDC	Technology	V_{dd}	# of ASIC Gates
Actel	RTAX2000S	0506	0.15µm CMOS Antifuse with 7 layers	3.3 V I/O; 2.5V Core	250,000
Actel	STAX1000S	0543	0.15µm CMOS Antifuse with 7 layers	3.3 V I/O; 2.5V Core	125,000

TABLE II
DUT TEST ARCHITECTURE

Device	String Nomenclature	Lot Date Code	Number of DFFs in Chain	Levels of Logic	Fan out to Enable
RTAX2000S	0F0L	0506	8000	0	No
RTAX2000S	0F0L	0506	800	0	No
RTAX2000S	4F4L	0506	2000	4	Yes
RTAX2000S	4F8L	0506	2000	8	Yes
RTAX2000S	0F0L	0506	1000	0	No
RTAX2000S	4F0L	0506	2000	0	Yes
RTAX1000S	4F8L	0543	700	8	Yes
RTAX1000S	0F0L	0543	700	0	No

validate the DFF contribution to the error cross-section. The enable logic fanned out to 4 DFF inputs and contained 4 levels of logic prior to the fan-out. Table I provides a description of the DUTs while Table II describes the DUT test architectures. The architectures are illustrated in Fig. 2. The chosen levels of logic (illustrated as bubbles pertaining to Fig. 2) were 0, 4, and 8 inverter gates.

The following nomenclature refers to the schematic in Fig. 3 and Fig. 4 (a description of the system level DUT to Tester interface). The DUT contains one clock input (CLK_SR_A) routed on HCLK. the hard-wired clock contained in the RTAX-S series of devices [2]. The clock is considered hardened by design and is able to reach every DFF clock pin within a maximum skew in the pico-seconds range (please refer to the device data sheet for chosen speed grade specifics). In order to follow a common synchronous design methodology, the reset input (CLR) within the DUT is connected to an Asynchronous Assert with a Synchronous De-assert (AASD) circuit [3]. System Reset is placed on the routed clock (following the AASD logic) and is connected to the CLR pin of every DFF (usage of the routed clock network ensures critical timing validation within synchronous circuitry and is a common approach to Actel FPGA design [10], [3]). There is one data input (D_SR). The four data outputs SCAN_DATA(3:0) are valid for 1 shift clock (SHIFT_CLK - data synchronizer to the tester).

In order to accommodate the large variation in clock frequencies, the following approach was taken to implement the DUT architecture. A 4-bit window (SCAN_DATA(3:0)) was placed parallel to the last 4-bits of the shift register. Every four clock cycles, the last 4-bits were shifted into the window. Since the upper bound of the system clock frequency was 150 MHz, the upper bound of the window loading frequency was 150 MHz/$4 = 37.5$ MHz. The data window along with a generated pulse (indicating data available, i.e., SHIFT_CLK) was fed to the tester. The SHIFT_CLK had the same frequency as the SCAN_DATA window.

At high frequencies, the internal CLK input to DFF (clock pin) latency can be longer than 1 clock period (skew is negligible but every node will have a similar latency)[2]. Due to this fact, other high frequency test-benches may have to reassemble (add or reduce hardware delays[5], or reconfigure the FPGA tester). The proposed window scheme provides data to the tester at slow enough speeds that it enables the data to be deterministically captured by the tester (i.e., all interface timing is synchronous and can be proven to be valid paths under all conditions). Not only does this method enhance the reliability of the captured data, but it also alleviates the need for reassembling the test-bench.

Although the test was bounded by 150 MHz, the same architectural approach can be implemented with much higher DUT system speeds. For example: Assume a 1 GHZ clock is the target DUT system frequency. Due to the deployment of the SHIFT_CLK, the tester does not have to take on the laborious task of synchronizing with the 1 GHZ clock—it only needs to edge detect a much slower SHIFT_CLK. If the window is expanded to 16 bits (SCAN_DATA(15:0)) with a system clock of

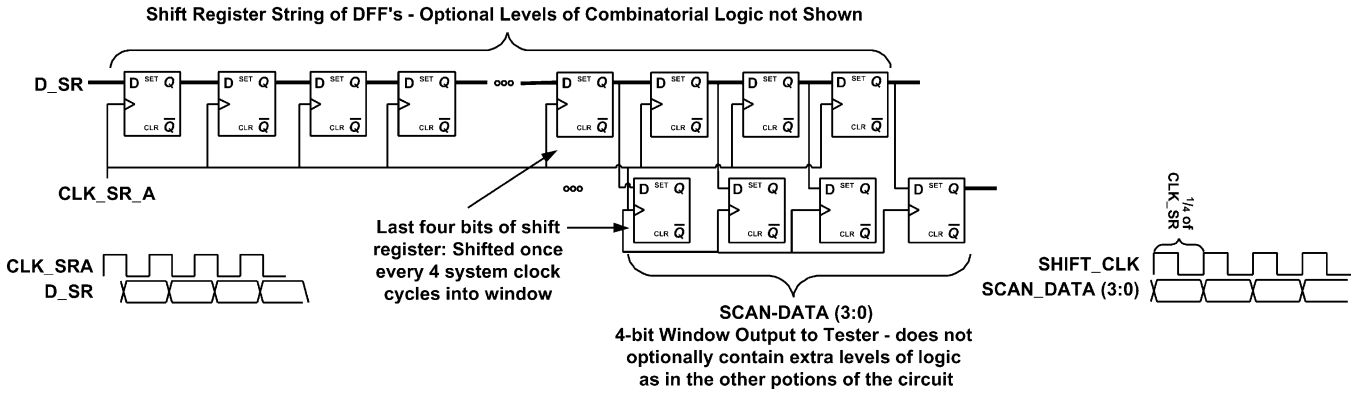

Fig. 3. Novel Window Architecture to Radiation Testing.

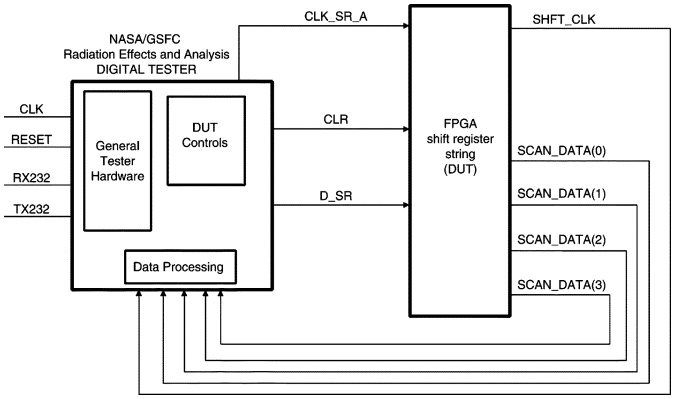

Fig. 4. Tester to DUT Schematic.

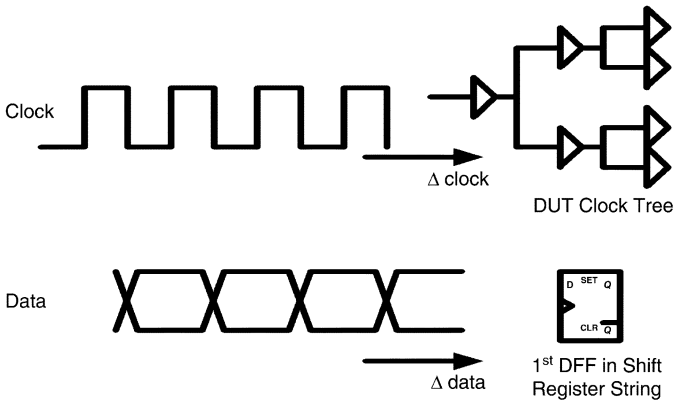

Fig. 5. Static Timing Analysis of Clock and Data Path.

1 GHZ, the task becomes feasible for the tester with a resultant SHIFT_CLK and SCAN_DATA frequency of 62.5 MHz.

III. Tester Implementation and Architecture

The NASA Goddard Radiation Effects and Analysis Group has developed a general tester board containing a Xilinx Spartan3 FPGA (low Cost Digital Tester—LCDT) [4]. This board supplies a 100 MHz Oscillator to the FPGA. Because of the reprogrammable Xilinx core, the tester has been successfully reused for several types of DUTs operating at various speeds. For the RTAX-S family testing, a Digital Clock Manager (DCM) is used to increase the system clock rate to 150 MHz. Due to the maximum speed of operation (150 MHz), the RTAX-S input control lines had to be carefully generated and had to undergo a rigorous static timing analysis. Please refer to Fig. 5.

The tester supplied the DUT with the following data patterns: static zero, static one, and alternating ones and zeros. The interesting consequence of the choice in patterns is that once the shift register has gone through the number of clock cycles equal to the complete size of the targeted shift register chain, the 4-bit window SCAN_DATA(3:0) will only change when a SEU occurs somewhere within the shift register chain. This is obvious for a pattern that is purely 0 or 1. However, if no error occurs while supplying an alternating pattern (based on how the pattern begins-either at 0 or 1), every fourth clock cycle the window statically remains at a value of “1010” or “0101”. Deployment of the windowing scheme with these test patterns reduces noise due to Simultaneously Switching Outputs (SSO). Due to potential SEUs in the DUT SHIFT_CLK generator circuitry, the tester has special logic to adjust to a pattern switching from a constant “1010” to a “0101” or visa versa.

IV. Test Setup, Results, and Analysis

The RTAX-S devices were irradiated with Argon, Copper, Krypton, and Xenon beams at 0 and 45 degrees at the Texas A&M University Cyclotron Radiation Effects Facility. Please refer to Table III for a list of ions and corresponding effective Linear Energy Transfer (LET) values. Faults from the RTAX-S devices were encountered at all LETs operating at 150 MHz. However, the number of SEUs was very low at an LET value of 8.5 MeV*cm ^{2}/mg.

A. Data Pattern Effects

In order to investigate data pattern effects, multiple architectures were analyzed at several LET values, and various frequencies for each data pattern. The following is demonstrated in Figs. 6(a) and (b). Analyzing across multiple architectures containing various numbers of transistors (combinatorial and

TABLE III
HEAVY ION TABLE

Ion	Energy (MEV/amu)	LET (MeV•cm²/mg) 0 deg	LET (MeV•cm²/mg) 45 deg
Ar	15	8.5	12
Cu	15	20.7	Not performed
Kr	15	28.5	40.26
Xe	15	52.7	74.5

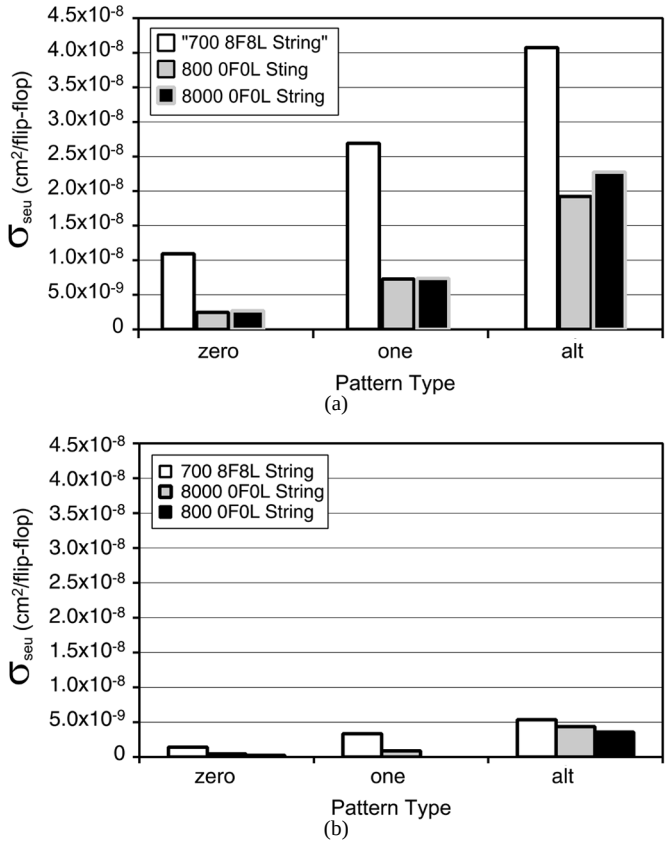

Fig. 6. (a) Data Pattern Effects at 150 MHz: 53 MeV*cm^2/mg. (b) Data Pattern Effects at 18.8 MHz: 53 MeV*cm^2/mg.

sequential) raises the question: is there a potential for an increased number of errors simply because there is an increased area of logic? To address this issue, separate shift register strings containing various numbers of DFF's and no combinatorial logic (i.e., just sequential logic): were irradiated and analyzed. Errors cross-sections per string were normalized (by DFF count), and then their associated, normalized error cross sections were compared. Figs. 6(a) and (b) illustrate the normalized error cross-sections of the 800 0F0L string (implemented in the RTAX2000S) and the 8000 0F0L string (implemented in the RTAX2000S) at 2 different frequencies. The normalized cross sections of the 800 and 8000 0F0L strings agree within statistical error. The following is the method used for normalized error cross-section calculation:

$$\sigma = \left(\frac{\text{err}}{\text{fluence}}\right)/\text{DFF} \tag{1}$$

σ	Normalized cross-section
Fluence	ions/cm ^{2}
DFF	number of Flip Flops in shift register string.

Static data input yielded lower error cross-sections than the alternating data pattern for all shift register strings. While comparing extreme cases (15 MHz 0F0L static 0-pattern to a 150 MHz 700 8F8L alternating-pattern), there is an order of magnitude difference in the error cross section. The results of the testing demonstrate the significance of data pattern and architectural choice. At higher frequencies, data paths that often change value can potentially have a higher susceptibility to transients and thus SEUs. The reason is due to the fact that transients are generated in "off" transistors (sensitive region). The number of "off" transistors is constant with static data patterns. However, during a particle strike, there exist possible race conditions (transistors turning on-off or off-on within a data path) as the state of data is flipping. During this transition period, the number of sensitive nodes is dramatically increased and thus the FPGA proves to be more susceptible to errors.

B. Architectural and Frequency Effects

The C-Cells are inverters and each C-Cell is an Actel primitive CM8 [2]. The CM8 can be configured as more complex functions and thus the inverter is a simplified implementation of the C-Cell. The inverter was chosen so that there would be no fanout within the data path and thus will simplify data analysis and will provide a relatively comparative data analysis to the previously taken NASA/Actel data set. This scheme of simplicity is limited due to the minimal cross section of a CM8 configured as an inverter. However, as a benefit there exists no fanout in the data and thus represents worse case (for this configuration) due to the lower capacitance at the node [7]).

At each LET, several tests were performed at various frequencies on all of the shift register string types. As the frequency increased, the error cross-section increased. Based on transient propagation and capture theory [1], [9], a shift register string containing hardened (TMR) DFFs and no combinatorial logic should not see a significant increase in its error cross section over frequency because, theoretically, DFF SEUs are not frequency dependent. However, the Actel DFF primitive (RCELL) within the RTAX-S series does contain combinatorial logic. This is where the frequency effects originate within the devices listed as containing no extra combinatorial logic [see the 0F0L data in Fig. 7(a)]. Fig. 7(a) demonstrates that there is a significant increase in transient susceptibility when adding C-Cells to a design. However, there is not a significant increase in error cross-section when changing the level of C-Cells from 4 to 8. This can be due to several reasons. Two are as follows: (1) the transients are unable to propagate through multiple levels of logic or (2) The CM8's implemented as inverters have a relatively small sensitive region and are clustered [2] such that the cross section of additional CM8's is overshadowed by the larger cross section of the transmit or receive buffer of each cluster. Further investigation into this phenomenon is necessary. It should include testing FPGA configurations: (1) containing additional variations of CM8 levels between DFFs (1, and 16 levels as an example) and (2) containing a new type

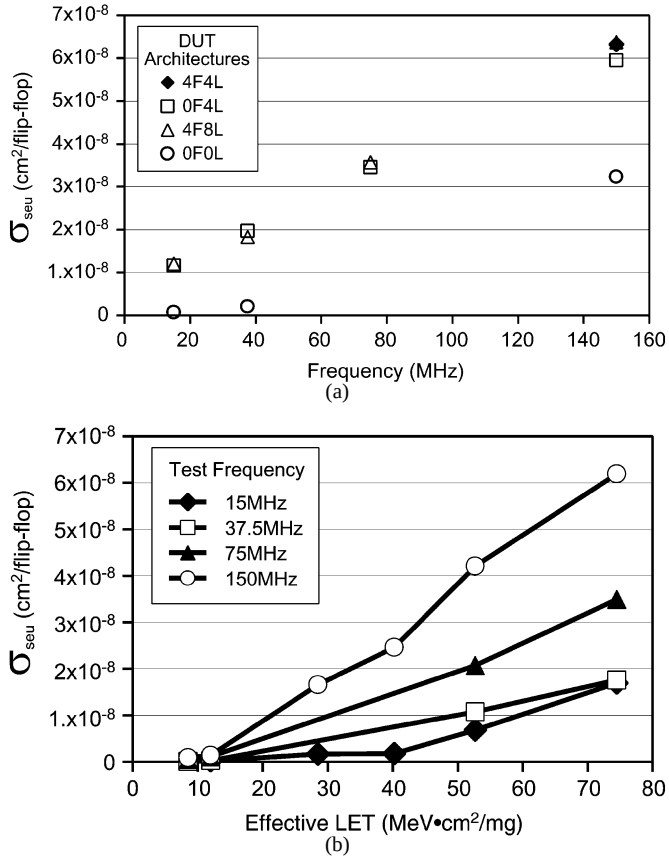

Fig. 7. (a) Cross Section vs. Frequency: Several Architectures with Alternating Pattern. (b) Effects of Frequency Response: 4F8L Alternating Pattern.

of string implemented with more complicated CM8 functionality (will need to have multiple strings and fanout within these designs—will increase the complexity of design from the relatively small cross-section of an inverter).

V. Bursts

Because of the synchronous nature of the tester, it is possible to capture and analyze high frequency DUT output data every clock cycle. Every fault is time stamped and a burst counter is incremented if there is a fault in consecutive clock cycles. This methodology of testing increases fault data detection and analysis. Time-stamped error data is sent out of the tester as it is received from the DUT via FIFO architecture. Thus during long bursts, the test will not stop unless commanded to do so.

RTAX2000S Data Bursts: Bursts only occur $\geq$ 75 MHz; no bursts $<$ 53 LET MeV*cm^2/mg.

RTAX1000S Data Bursts: No Burst observed $\leqslant$ 75 LET MeV*cm^2/mg.

Bursts occurring within the 2000 S series were of variable lengths ranging from double-digit consecutive cycles to values larger than the actual string length. Bursts larger than the actual string length suggest that one of the DFFs that control the AASD reset circuitry was hit and thus the entire string is reset. Double Digit bursts that were smaller than the actual shift register chain suggest that a buffer within the reset tree was hit and only a portion of the tree had been reset.

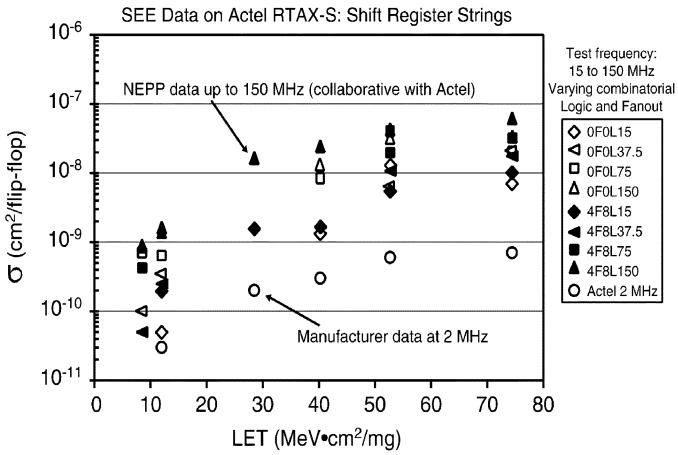

Fig. 8. LET vs. Error Cross-Section for Multiple Architectures at Multiple Frequencies. Data Demonstrates Frequency Response Variation across Architectures. Data Pattern = Alternating.

VI. Flip-Flop Error Rate Calculations

Flip-flop error rates were calculated using the CREME96 environment for geostationary orbit (GEO) and solar minimum conditions. The shape parameters for the design with the largest number of combinatorial logic operating at the highest test frequency were as follows:

- Shape Parameters: $\sigma_{\text{device}} = 1.1 \times 10^{-4}$ cm^2, LET onset = 5 MeV* cm^2/mg, $\mathrm{W} = 35, \mathrm{S} = 2, \text{funnel} = 0$, and $\text{Depth} = 2$ microns.
- Device setup: 150 MHz and 8 extra levels of combinatorial logic (4F8L) $<$ 5 $\times$ 10-8 errors/flip-flop/day.

The shape parameters for the design implemented with only RCELLs operating at the slowest test frequency were as follows:

- Shape Parameters: $\sigma_{\text{device}} = 2.0 \times 10^{-5}$ cm^2, LET onset = 5MeV* cm ^{2}/mg, $\mathrm{W} = 30, \mathrm{S} = 1, \text{funnel} = 0$, and $\text{Depth} = 2$ microns.
- Device setup: 15 MHz and no extra levels of combinatorial logic (0F0L) $<$ 5.6 $\times$ 10-9 errors/flip-flop/day.

The results show a significant difference compared to the Actel reported data sheet value of $< 4 \times 10^{-11}$ errors/flip-flop/day. Discrepancy between our data and previously reported Actel data is primarily due to the new test structure's architecture (both tester and DUT) that permits reliable high frequency operation.

VII. Conclusion

A novel approach to variable and high frequency SEU testing was implemented. The DUT was operable at 4-times the data capture rate which made high speed data capture feasible (without concerns of inaccurate data encapsulation) and automated. The results of the testing demonstrated both frequency effects and combinatorial architectural effects. Combining the data indicates that the majority of errors in a hardened anti-fuse device will originate as transients and at high frequencies will become SEUs. This research has clearly proven that as technology is evolving the development of new approaches to SEU testing is a necessity in order to accurately characterize a device.

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